

**Claims**

1. Arrangement for adaptive bit recovery including an adaptive equalizer (13) and an adaptive partial response maximum likelihood detector (14), **characterized** in that the arrangement further includes an overflow control block (86) for the adaptive equalizer (13) for monitoring one or more of the adaptation coefficients.
2. Arrangement according to claim 1, **further** including a scaling block (89) for applying a scaling to one or more of the data paths of the coefficient values when the overflow control block (86) indicates that one or more of the coefficients run out of their intended data range.
3. Arrangement according to claims 1 or 2, **further** including means (87) for obtaining phase information by comparing the highest absolute coefficient value with its coefficient number.
4. Arrangement according to one of claims 1 to 3, **further** including a control logic (74) for an adaptation constant for a tap value update for the coefficients.
5. Arrangement according to claim 4, **further** including a gradient analyzing block (76) for analyzing a gradient of the coefficient transitions for monitoring the speed of adaptation.
6. Arrangement according to claim 5, **further** including a set level block (77) for performing an adaptation coefficient scaling in dependence on the value of the detected gradient.
7. Arrangement for adaptive bit recovery including an adaptive equalizer (13) and an adaptive partial response maximum likelihood detector (14), **characterized** in that the arrangement further includes a state violation checker (162) for monitoring the allowed states and indicating state

violations, and a noise detector (155) for detecting larger deviations of the target values.

8. Arrangement according to claim 7, **further** including a  
5 controllable scaling block (163) for scaling the target value update to reduce the impact of input sample changes.

9. Arrangement according to claim 7 or 8, **further** including a  
10 path memory and survivor control block (153) for storing path decisions for each state and the most likely state.

10. Arrangement according to claim 9, **further** including an output checker (175) for finding invalid bit transitions.

15 11. Arrangement according to one of claims 1 to 10, **wherein** generated error information is provided to further processing units (9) for supporting data processing.

20 12. Apparatus for reading from and/or writing to recording media, **characterized** in that it includes an arrangement according to one of claims 1-11 for adaptive bit recovery.